445/78, 82, 83 ✓ 362.1 375.7

455/423, 424, 425

Listings of Claims

1 - 4 (cancelled)

A1

5. (new) A method of verifying the functionality of a circuit comprising:

providing a design level circuit with a plurality circuit blocks in communication with signal paths and input and output terminals;

providing a test input signal at the input terminal, the test input signal causes the circuit to produce a test output signal at the output terminal; and

comparing the test output signal with an expected output signal to verify the functionality of the circuit

6. (new) The method of claim 5 wherein providing a design level circuit comprises providing a design level circuit in VHDL.

7. (new) The method of claim 6 wherein providing a design level circuit comprises providing a design level communication circuit.

8. (new) The method of claim 6 wherein design level circuit comprises normal and test modes, wherein in test mode, circuit blocks can be selectively tested.

9. (new) The method of claim 5 wherein providing a design level circuit comprises providing a design level communication circuit.

10. (new) The method of claim 9 wherein design level circuit comprises normal and test modes, wherein in test mode, circuit blocks can be selectively tested.

11. (new) The method of claim 5 wherein design level circuit comprises normal and test modes, wherein in test mode, circuit blocks can be selectively tested.

12. (new) The method claim 1 wherein the design level circuit comprises select switches for selectively decoupling circuit blocks not tested from the signal paths and selectively coupling circuit blocks which are tested to the signal paths.

A1 Concl'd

13. (new) The method of claim 1 further comprises providing the design level circuit with a test switch for coupling signal paths together to create a test signal loop for the test input signal.

14. (new) The method of claim 13 whercin the test input signal comprises a radio frequency signal, or a sine or a square wave.

15. (new) The method of claim 13 wherein the design level circuit comprises select switchcs for selectively decoupling circuit blocks not tested from the signal paths and selectively coupling circuit blocks which are tested to the signal paths.